What we claim is:

1. A signal processing apparatus for assigning channels, to be used, to a plurality of DSP's comprising:

a control circuit for controlling the DSP's,

a library for storing a plurality of signal processing algorithms, and

a channel assignment table,

the control circuit, when an assignment designation of a channel and an algorithm for each of the DSP's is received, comparing the designated algorithm with the algorithms having been already downloaded to the DSP's based on the table, thereby downloading only an algorithm required to be newly downloaded from the library to the DSP's or between the DSP's and assigning the downloaded algorithm to the received channel.

2. The signal processing apparatus as claimed in claim 1 wherein the channel assignment table fixedly stores a relationship between channels in use and the DSP's, and the control circuit detects a DSP corresponding to the designated channel by referring to the table and newly downloads the designated algorithm from the library for the DSP.

3. The signal processing apparatus as claimed in claim 2 wherein the channel assignment table fixedly stores the relationship between the channels and processing positions, and the control circuit starts up the algorithm at an empty processing position in assigned processing positions by referring to the table for the DSP to which the algorithm is newly downloaded.

4. The signal processing apparatus as claimed in claim 1 wherein the channel assignment table variably stores a relationship between the channels in use and the DSP's, and in case a DSP exists which has already downloaded the designated algorithm and which has an unused channel, the control circuit uses the algorithm of the DSP and

updates the table.

5. The signal processing apparatus as claimed in claim 1 or 4 wherein the channel assignment table variably stores the relationship between the channels in use and the DSP's, and in case a DSP exists which has already downloaded a designated algorithm and which has no unused channel, the control circuit newly downloads the algorithm from the DSP to a different DSP, and updates the table.

6. The signal processing apparatus as claimed in claim 1 wherein the channel assignment table variably stores a relationship between the channels in use, the DSP's, and processing positions, and in case a DSP exists which has already downloaded the designated algorithm and which has an empty processing position, the control circuit newly downloads the algorithm from the DSP, and updates the table.

7. The signal processing apparatus as claimed in claim 1 or 6 wherein the channel assignment table variably stores the relationship between the channels in use, the DSP's, and the processing positions, and in case a DSP exists which has already downloaded the designated algorithm and which has no empty processing position, the control circuit newly downloads the algorithm of the DSP to a different DSP, and updates the table.

8. The signal processing apparatus as claimed in claim 5 or 7 wherein the control circuit selects a DSP which has downloaded an algorithm with a lower priority as the different DSP.

9. The signal processing apparatus as claimed in claim 6 or 7 wherein the control circuit starts up the downloaded algorithm at an assigned processing position.

10. The signal processing apparatus as claimed in any one of claims 1 to 9 wherein the control circuit has initially downloaded an identical algorithm to the DSP's.

11. The signal processing apparatus as claimed in any one of claims 1 to 9 wherein the control circuit has initially downloaded different

algorithms to the DSP's.

12. The signal processing apparatus as claimed in claim 4 or 5 wherein the control circuit has preliminarily downloaded an algorithm with a highest priority within algorithms not downloaded to DSP's in which empty channels have occurred.

13. The signal processing apparatus as claimed in claim 4 or 5, further comprising an assignment history table,

the control circuit updating the assignment history table at a time of assignment completion of algorithms, and preliminarily downloading an algorithm with a highest usage frequency within algorithms not downloaded, from the assignment history table, to DSP's in which empty channels have occurred.

14. The signal processing apparatus as claimed in claim 6 or 7 wherein the control circuit has preliminarily downloaded an algorithm with a highest priority within algorithms not downloaded to DSP's in which all of the processing positions have become empty.

15. The signal processing apparatus as claimed in claim 6 or 7, further comprising an assignment history table,

the control circuit updating the assignment history table at a time of assignment completion of algorithms, and having preliminarily downloaded an algorithm with a highest usage frequency within algorithms not downloaded, from the assignment history table, to DSP's in which all of the processing positions have become empty.

16. The signal processing apparatus as claimed in any one of claims 1 to 15 wherein the channel comprises a voice channel, the DSP includes a voice encoding/decoding device, and the algorithm comprises a processing program.

17. The signal processing apparatus as claimed in any one of claims 4 to 16, further comprising a channel assignment controller for executing a channel assignment under control of the control circuit.